AMENDMENTS

IN THE ABSTRACT:

Clock pulse generator apparatus comprising a clock pulse generator ~~(CLK)~~ for generating a train of primary clock pulses having leading and trailing edges. A delay line ~~(14)~~ produces a train of delayed clock pulses ~~(CLK_D)~~ presenting delayed edges whose timing relative to corresponding edges of the primary clock pulses ~~(CLK)~~ is defined by the delay line. A logic circuit ~~(15)~~ produces a train of combined clock pulses ~~(CLK_JF)~~ presenting leading and trailing edges defined alternately by one of the delayed edges and the corresponding edge of the primary clock pulse, so that the combined clock pulses comprise active clock phases ~~(ACP)~~ having widths defined by the delay line; the variability of the widths of the active clock phases ~~(ACP)~~ is smaller than the variability of the positions of the leading and trailing edges of the primary clock pulses ~~(CLK)~~. ~~The active clock phases (ACP) alternate with non-active clock phases (NACP) whose widths vary as a function of variation in the positions of the primary clock pulses (CLK) and absord those variations. The delay line (14) comprises a series of cascaded, substantially identical delay elements (16). A temperature and process variation circuit (22) is also described.~~

~~Application especially to continuous-time sigma-delta converters where a critical integrator (2; 10) integrates a signal over periods of time defined by the widths of the active clock phases (ACP).~~

~~Figures 6 & 8~~